

Notice of References Cited

Application/Control No.

09/608,158

Applicant(s)/Patent Under
Reexamination
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2123

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,038,020	03-2000	Tsukuda	356/237.5
	B	US-			
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	F	US-			
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	I	US-			
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	K	US-			
	L	US-			
	M	US-			

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Axelrad, V. et al., "Efficient full-chip yield analysis methodology for OPC-corrected VLSI designs", IEEE, March 2000.
	V	Balasinski, A et al., "A novel pproach to simulate the effect of Optical Proximity on MOSFET parametric yield", IEEE, December 1999.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.